# Translating Modelica to HDL: An Automated Design Flow for FPGA-based Real-Time Hardware-in-the-Loop Simulations


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Recent movement towards electric vehicles imposes new challenges on the development of drivetrains. Especially the verification of electric motor controllers (EMCs) using the hardware-in-the-loop (HiL) test methodology requires real-time simulation of the functional environment with low latencies. An electric motor emulator (EME) emulates an electrical motor under real conditions, including position feedback and other sensor signals. If needed, a power stage recreates the original currents and voltages. Due to the dynamic electric behavior of the motor, the model iteration rate has to be in the order of one microsecond. Since such real-time requirements are hard to meet using software solutions, HiL emulators of electric machines typically involve a field-programmable gate array (FPGA) which carries out time-critical computations. Although Modelica has proven to be an effective language for describing electric hybrid drivetrains [1], there is currently no tool support for compiling Modelica to FPGAs.

We present an integrated methodology which translates Modelica models to VHDL hardware designs. The implementation is realized and validated using SimulationX. Our approach combines well-known methodologies from both differential-algebraic equation (DAE) processing and high-level synthesis (HLS) [2]. We employ inline integration [3] to obtain a compact calculation rule which can be efficiently mapped to hardware. Moreover, we incorporate parametrizable circuit templates (so-called IP cores) to solve common subproblems during the mapping process. The combined model of motor and drivetrain is built using an FPGA-aware Modelica library. The resulting model is automatically transformed to an FPGA design, traversing a sequence of transformation steps, such as compilation, assignment of operations to FPGA clock steps (scheduling), assignment of operations to hardware resources (allocation and binding), interconnect and control path construction. We demonstrate the methodology using the example of a direct current (DC) motor. Our results show that the generated hardware design meets the given time and resource requirements.


## References


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