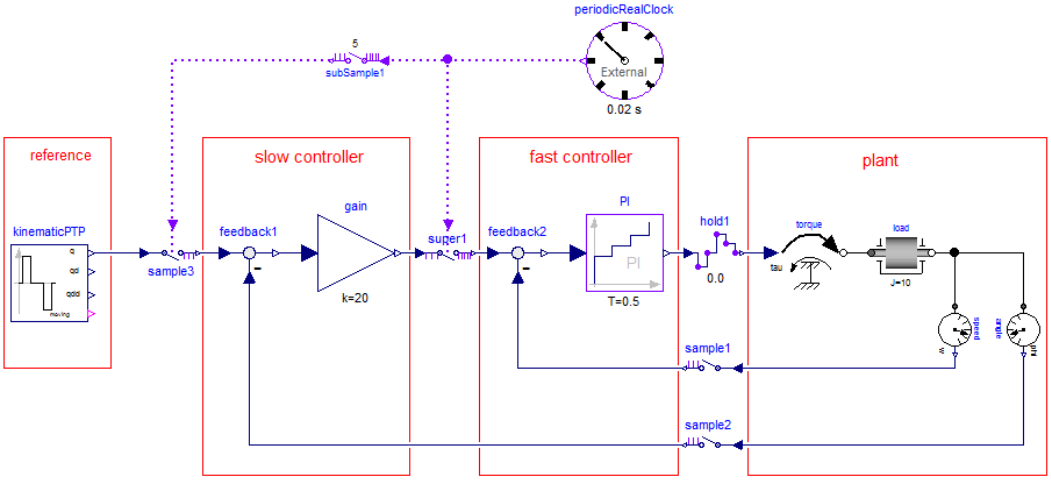
A Library for Synchronous Control Systems in Modelica

Martin Otter[1], Bernhard Thiele[1], Hilding Elmqvist[2]
[2]DLR Institute of System Dynamics and Control, Wessling, Germany
[1]Dassault Systèmes AB, Ideon Science Park, SE-223 70 Lund, Sweden
Martin.Otter@dlr.de, Bernhard.Thiele@dlr.de, Hilding.Elmqvist@3ds.com,

In the Modelica language version 3.3 synchronous language features have been introduced to precisely define and synchronize sampled data systems with different sampling rates. This article is a companion paper to (*Elmqvist et.al. 2012*) which should be first inspected to understand why new language elements have been introduced, as well as the syntax and semantics of them.

In order to utilize these language elements in an actual model in a *convenient way*, a free library "Modelica_Synchronous" has been developed using a prototype of Dymola for the new language elements. This library is in a prototype status. After an evaluation period it is planned to include this library into the Modelica Standard Library. Note, all Modelica libraries designed so far for sampled systems, such as Modelica.Blocks.Discrete, Modelica_LinearSystems2.Controller and Modelica_EmbeddedSystems are becoming obsolete and should be replaced by this new library.

A typical, simple example to define sampled data systems with this library is shown in the screen shot below, consisting of a continuous-time load inertia, and a position and speed controller with two sample rates that are precisely time synchronized to each other. The blocks `sample1`, `sample2`, and `sample3` sample a continuous time signal and provide them as clocked, discrete-time signals. The block `hold1` is a zero-order hold and transforms a clocked signal to a continuous time signal. The block `super1` defines that its input is super-sampled and provided as output. All equations in a partition marked by `sample`, `hold`, `superSample` (and blocks `subSample`, `shiftSample`, `backSample`) form a partition that is associated exactly to one clock (e.g. a clock with a periodic sample rate). The equations of a clocked partition are automatically deduced by clock inference using the simple rule that all variables used in an equation (with exception of the first arguments of the above operators that mark the boundaries of a partition) must belong to the same clock. Clocks can then be associated to partitions as optional inputs to the boundary marking blocks. Below, the fast controller has a sample rate of 0.02 s and the slow controller of 5*0.02 = 0.1 s.



References

Elmqvist H., Otter M., and Mattsson S.E. (2012): **Fundamentals of Synchronous Control in Modelica**. Proceedings of 9th Int. Modelica Conference, Munich, Germany, Sept. 3-5.